ABSTRACT

A semiconductor device having an electrically erasable programmable read only memory (EEPROM) comprises a contactless array of EEPROM memory cells disposed in rows and columns and constructed over a silicon-on-insulator wafer. Each EEPROM memory cell comprises a drain region, a source region, a gate region, and a body region. The semiconductor device further comprises a plurality of gate lines each connecting the gate regions of a row of EEPROM memory cells, a plurality of body lines each connecting the body regions of a column of EEPROM memory cells, a plurality of source lines each connecting the source regions of a column of EEPROM memory cells, and a plurality of drain lines each connecting the drain regions of a column of EEPROM memory cells. The source lines and the drain lines are buried lines, and the source regions and the drain regions of a column of EEPROM memory cells are insulated from the source regions and the drain regions of the adjacent columns of EEPROM memory cells.